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DSP Solutions for Industry & Research

HSMC DVI 1080P SDRAM Loop-through Reference Design

Version 0.1

Revision history

Version	Comment
V0.1	Beta release

Introduction

The DVI Loop-through demo is intended as a basis for developers to quickly implement full HD 1080P video processing designs. A simple video pipeline is presented which takes a Full HD video signal from the HSMC DVI Input port and passes it through two, triple frame buffers.

Image buffering is a fundamental requirement for many video processing pipelines in which the input and output images are unsynchronised. Such applications include up/down scaling or image combining.

The first stage is used to synchronise the input video stream to the local pipeline video clock through the triple frame buffer. The second buffer is not normally required as the FPGA is able to process the incoming pixel stream at the full HD clock rate and output the processed data directly to the VGA output port. The second stage is included for demonstration purposes.

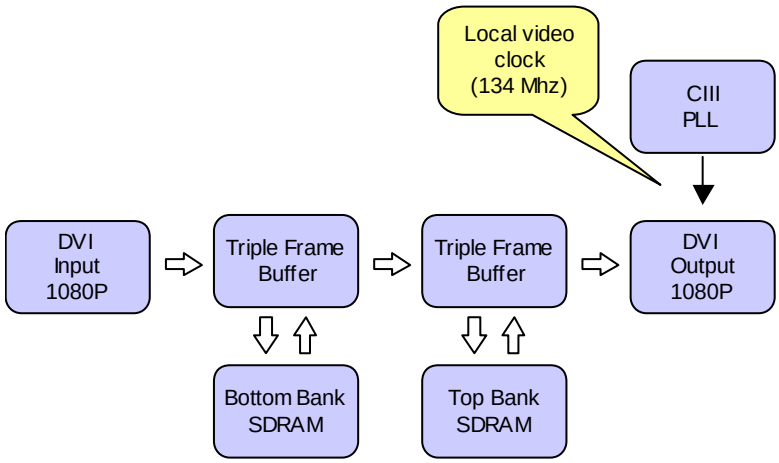

Figure 1

After the first triple frame buffer the video signal is now relative to the local SoPC system clock. This is where a developer's video pipeline can be introduced. See Figure 2.

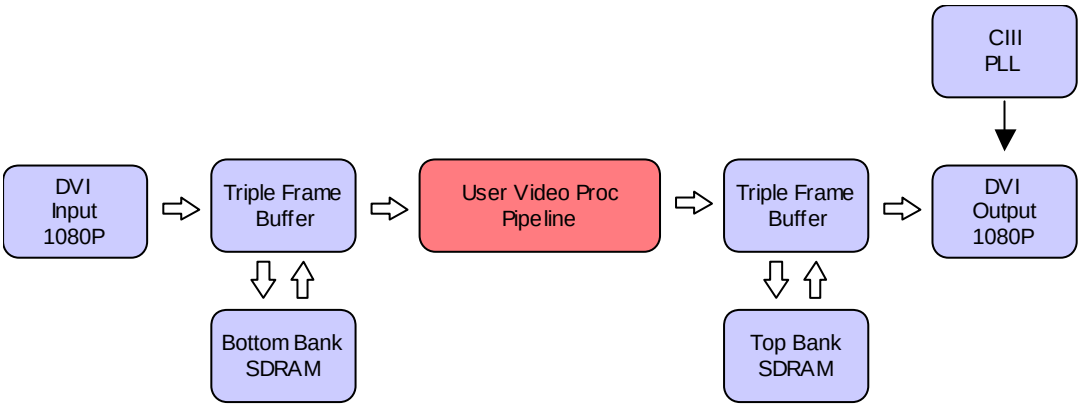

Figure 2

The SoPC builder is shown below. The two DDR2 memory banks run at 166Mhz and the local SoPC system clock is set to the bottom bank sys clock to avoid the need for two clock crossing bridges.

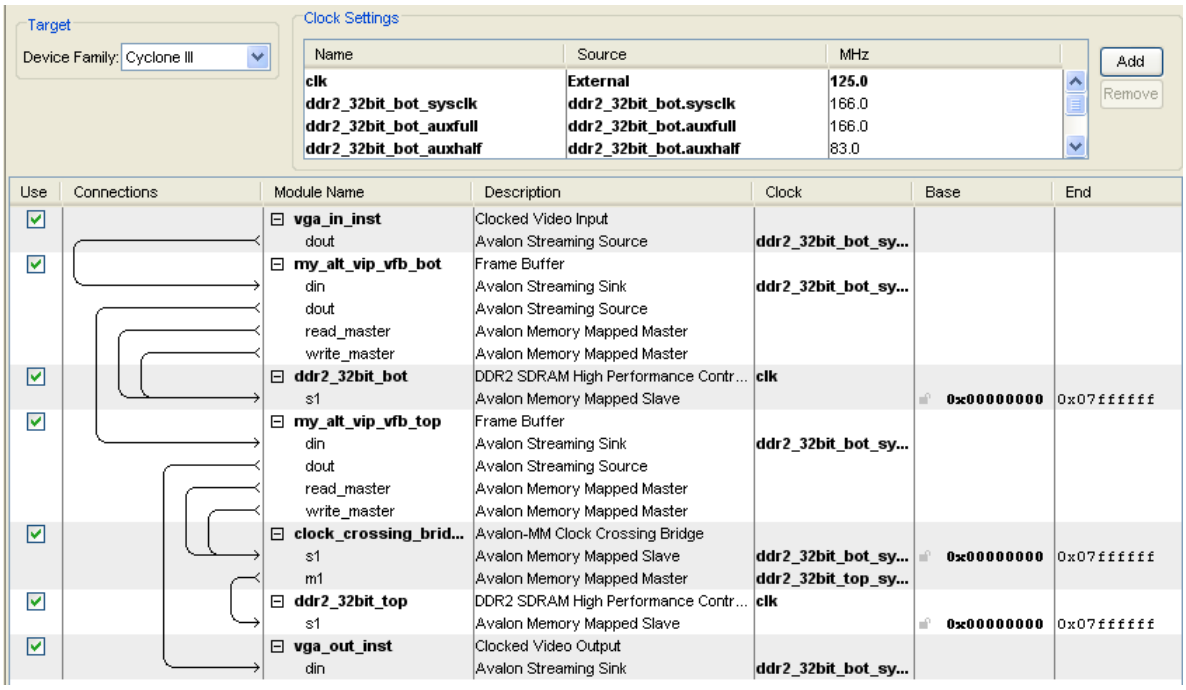

Figure 3

Installation

To run the design it is first necessary to obtain the source files and restore the Quartus Archive (QAR) file into a chosen directory.

A 1080P video source and capable display is required to run the demonstration. For correct operation it is necessary to configure the video test signal to have positive polarity on both the vertical and horizontal sync signals.

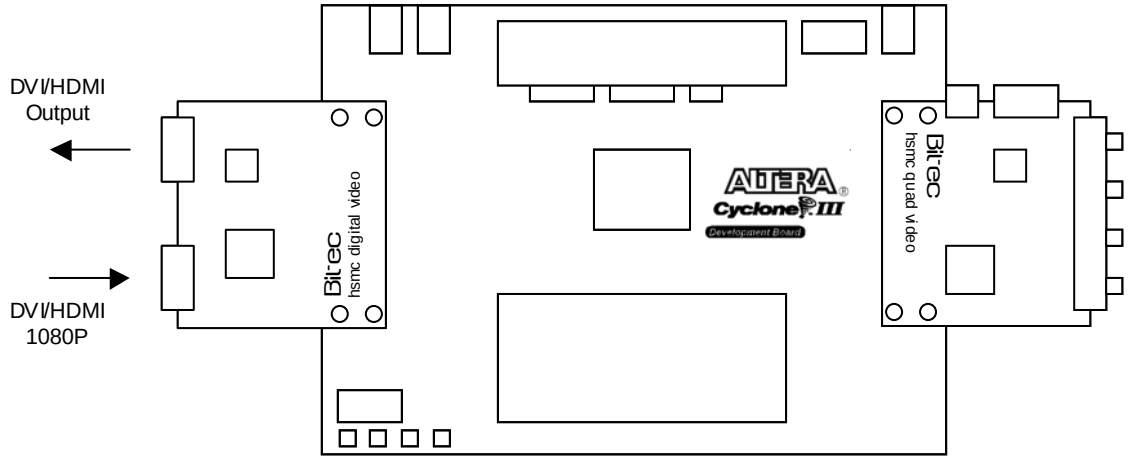

Figure 4

Once the hardware and software are ready, the sof file must be downloaded into the target Dev Kit board.

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