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DSP Solutions for Industry & Research

CIII VDK Picture-in-Picture (PiP) Reference Design

Version 0.1

Revision history

Version	Comment
V0.1	Beta release

Introduction

Found primarily on more expensive televisions, PIP lets you watch a second video stream in a little window. More-elaborate versions can resize the window, move it around the screen, create still or multiple still images, or simply divide the screen into two same-size pictures, often called 'picture-outside-picture' (POP).

This reference design demonstrates the use of the Bitec CIII VDK for picture-in-picture on 1080P Full HD video signals. A single composite/s-video channel is combined with a Full HD 1080P video stream to generate a 1080P, PiP output video stream. The resulting image stream is the combination of both input video signals.

A block diagram of the SoPC is shown in Figure 1. Both the input video signals are triple frame buffered to allow synchronization to the output video stream driven by the local 134Mhz pixel clock.

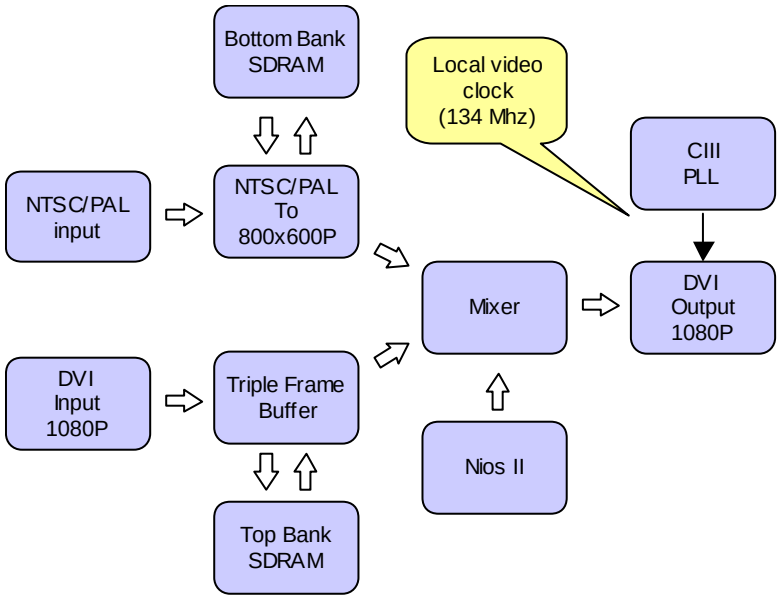


Figure 1 Picture-in-picture block diagram

Detail of the conversion between NTSC/PAL to 800x600P is shown in Figure 2. The input signal is first converted from YCrCb to RGB. The resulting RGB

interlaced image stream is then converted to a progressive image stream through the de-interlace component. The progressive image stream is then scaled to 800x600 before triple buffering.

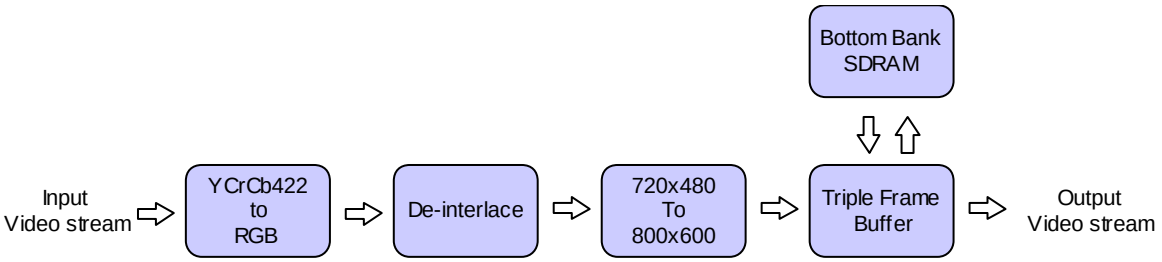


Figure 2 NTSC/PAL to 800x600P video pipeline block diagram

The mixer component is responsible for combining the two image streams. This component has a Nios II control port to allow run time changes to the mixer behaviour. In this reference design the PiP sub-picture coordinates are continuously changed by the Nios II thus moving the PiP around the background 1080P video in real-time.

The SoPC builder can be seen in Figure 4. The complete video pipeline is displayed showing the clocking signals used throughout the design. Each pipeline is assigned a colour for clarity. The composite video pipeline is coloured in blue, the 1080P signal is green and the combined image in red.

The system is clocked at the DDR2 bottom bank clock rate. A single clock crossing bridge is necessary to access the DDR2 top bank component used to triple buffer the 1080P video stream.

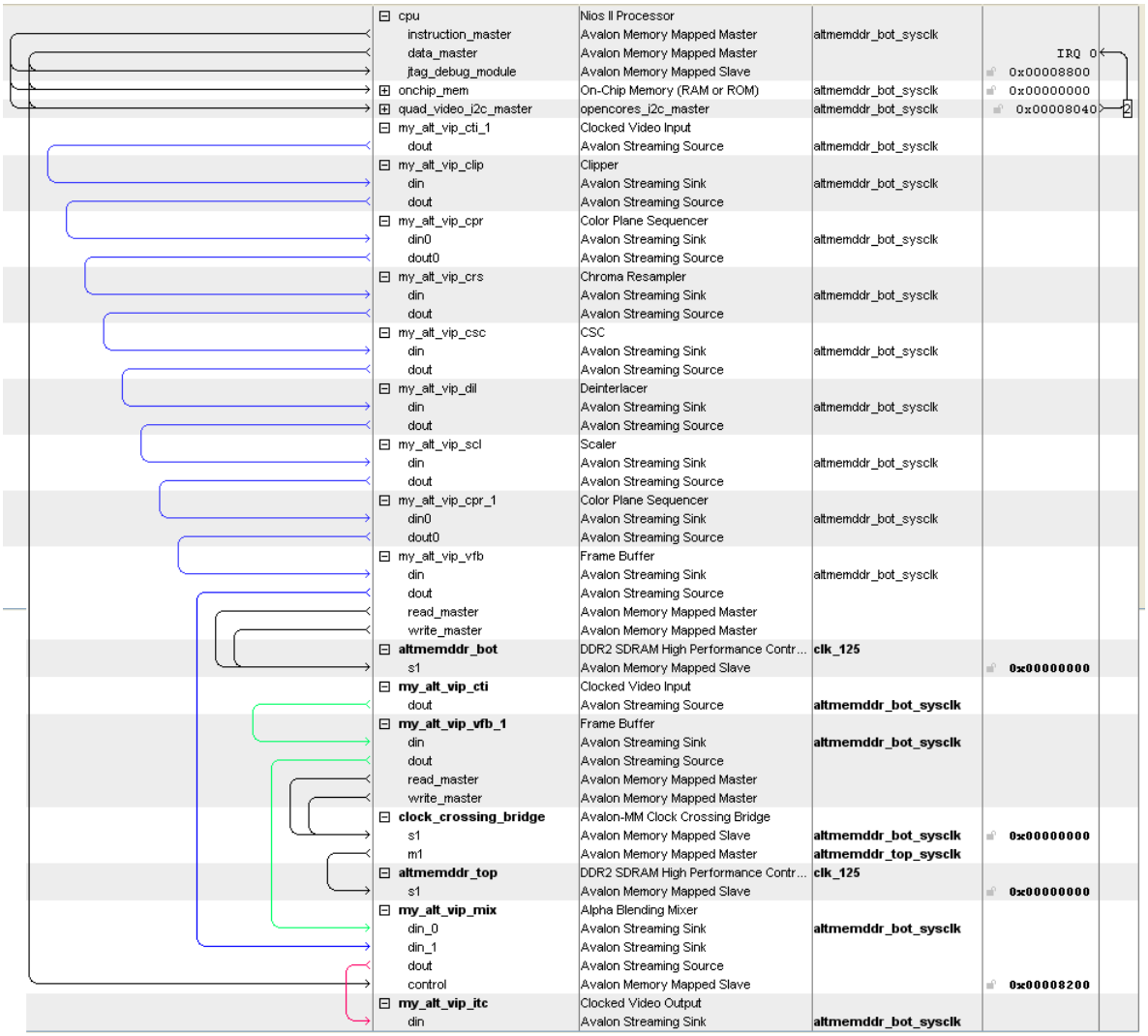


Figure 3 PiP SoPC builder

Installation

The hardware configuration is shown in Figure 4. A 1080P video source and composite video source are required. A PC DVI or HDMI video signal can be used for the demo. The composite signal can be any NTSC/PAL video signal.

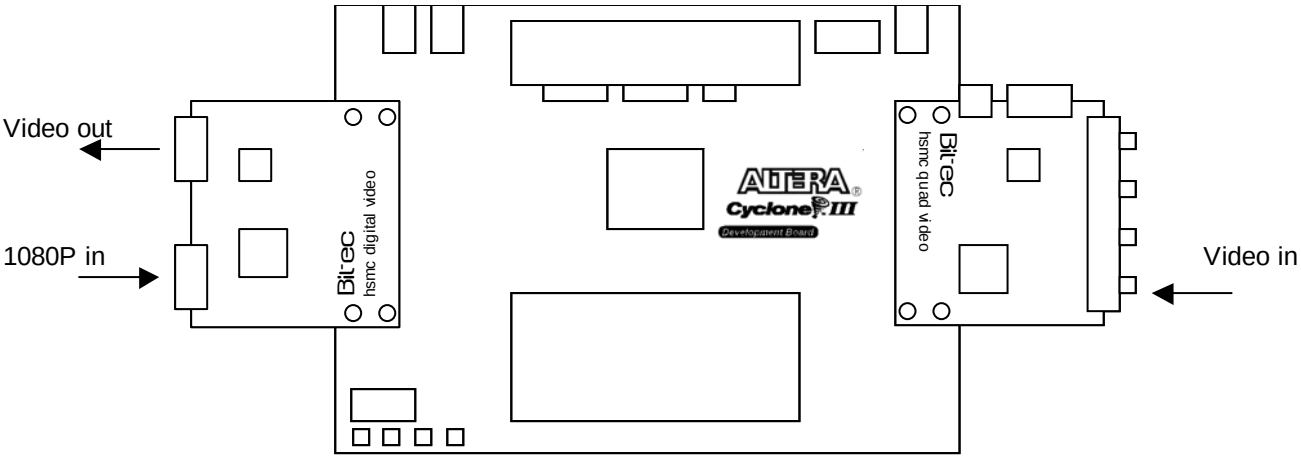


Figure 4 Hardware configuration

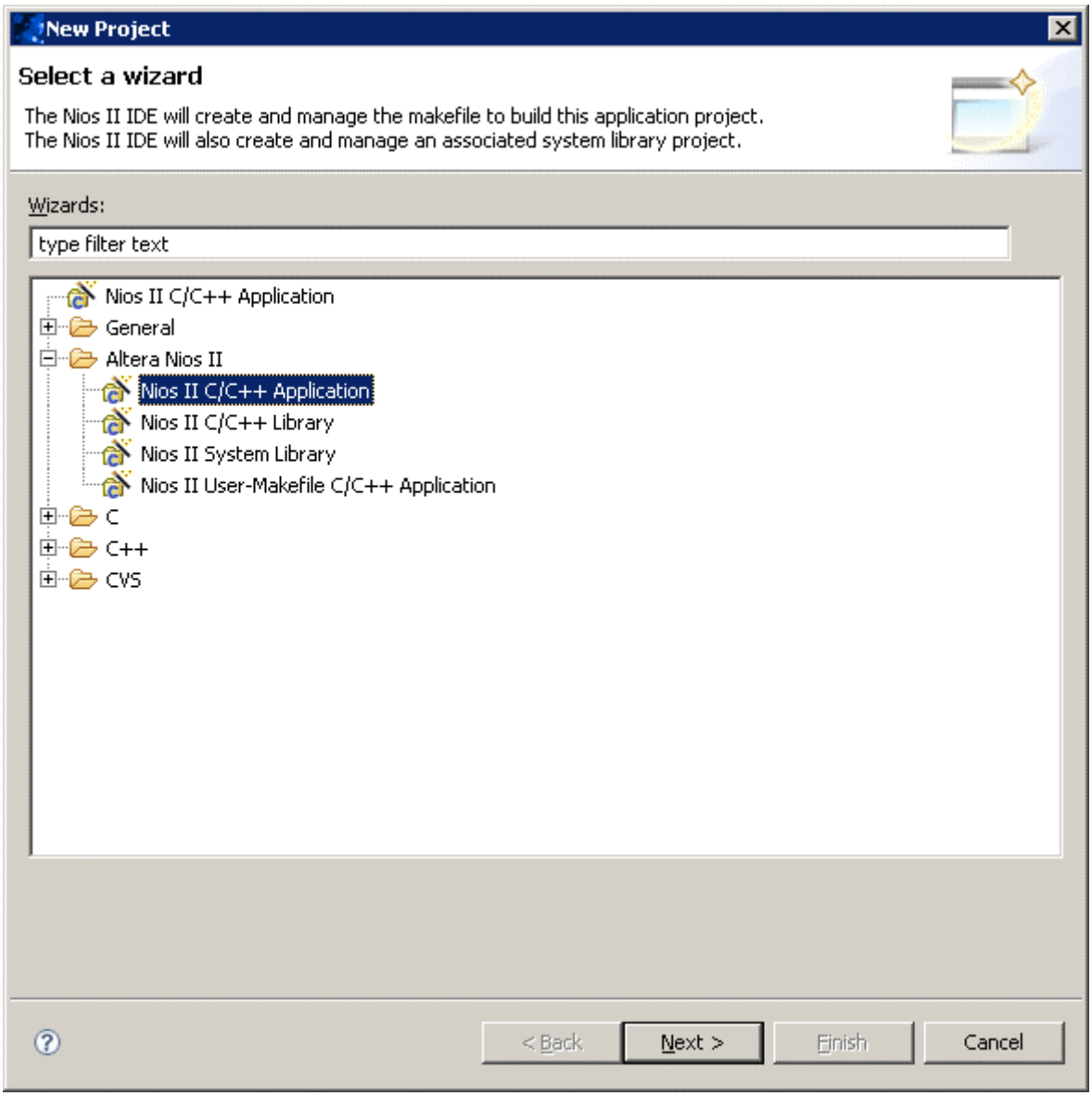
The demo Nios II software executes from onchip memory and will run when the FPGA SOF file is downloaded. The steps necessary to re-build the software are detailed below.

Building the demo software

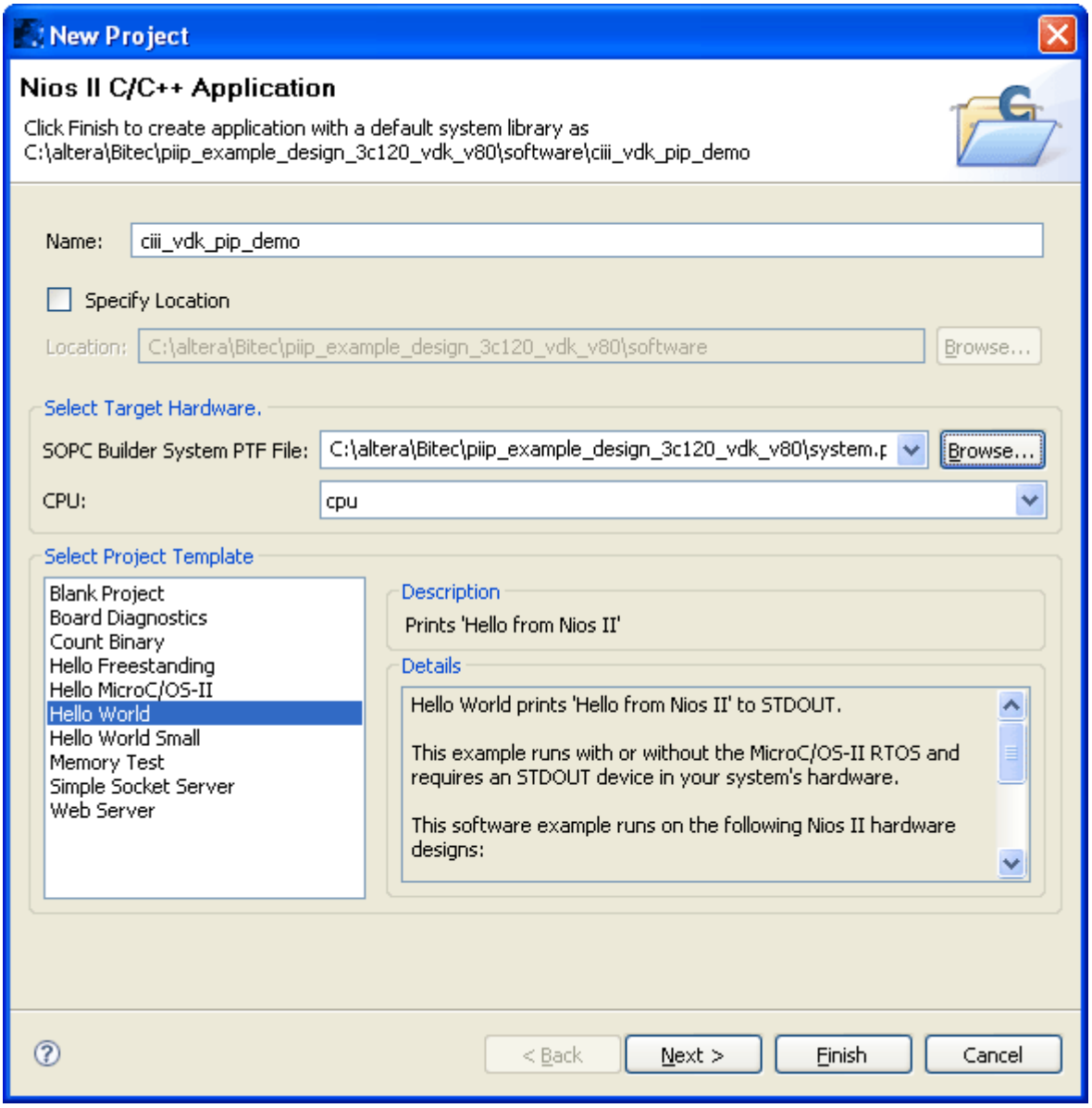
Before executing the demo software it is first necessary to create a Nios II project and include the supplied source files.

Open the Nios II IDE and "Switch Workspace" to the "Software" directory.

Create a new "Nios II C/C++ Application" from the File->New menu.



Change the project name to ciii_vdk_pip_demo and choose the SOPC Builder System PTF to select the system.ptf demo Nios II processor description file.



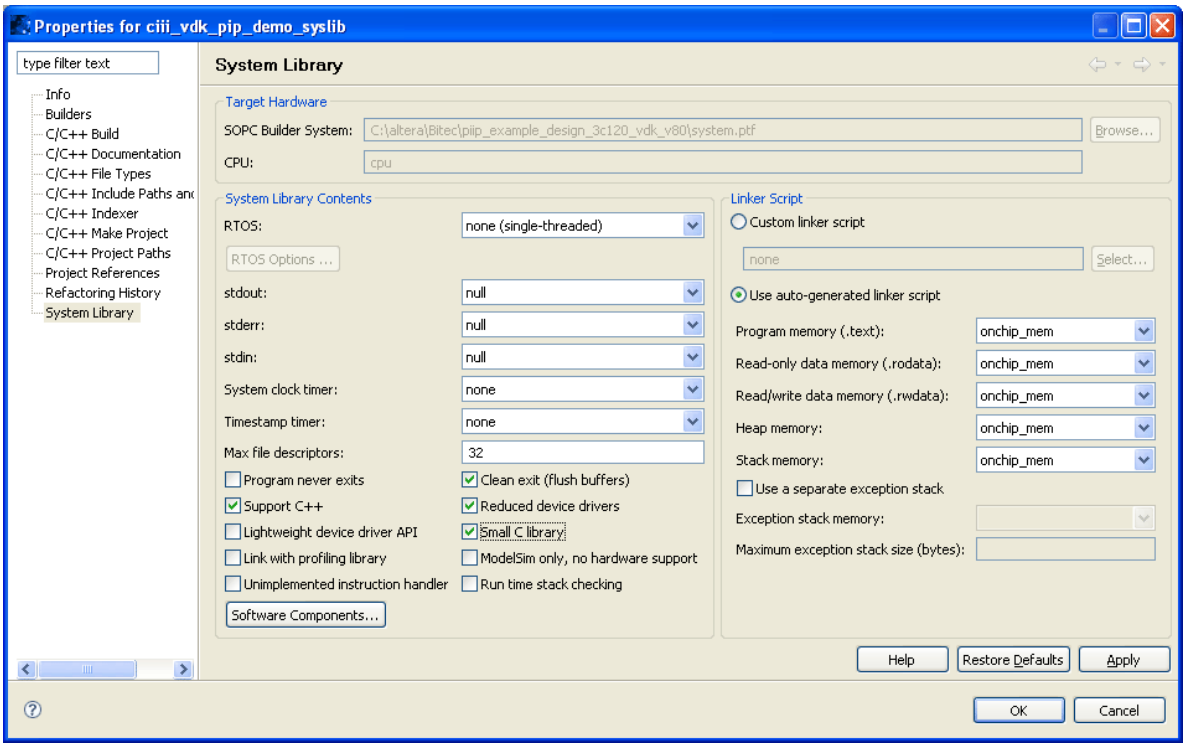
Click “Next” and then “Finish”. Two directories will be created below the Software directory.

Copy the supplied source files into the newly created “ciii_vdk_pip_demo” directory.

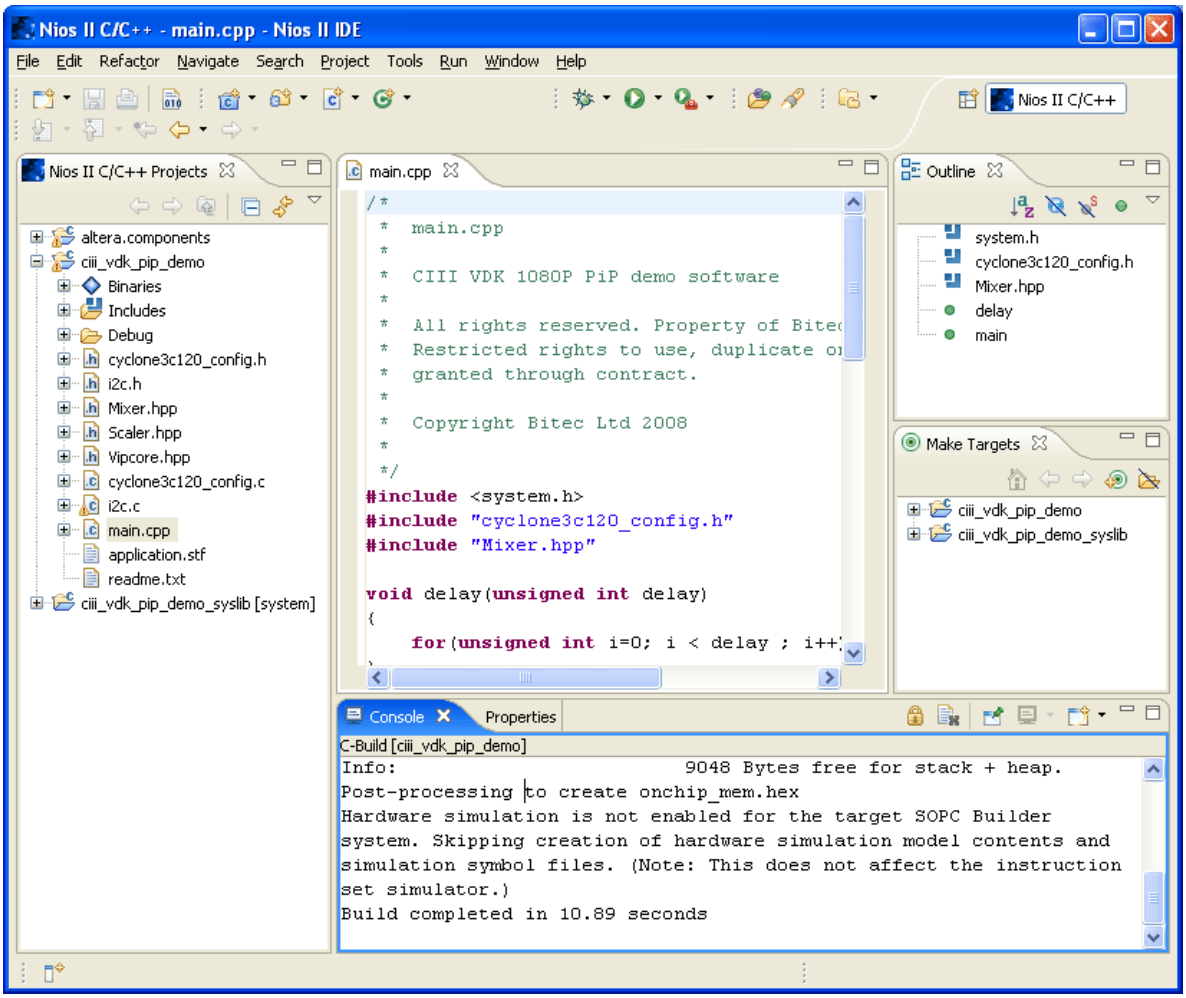
Highlight the ciii_vdk_pip_demo directory in “Project Browser” pane “Refresh” using F5 or File->Refresh.

Select the auto generated hello_world.c and delete.

Before building, set the memory options to “onchip_mem” in the system library properties. Also select the “Reduced Drivers” and “Small C Library” options.



The project is now ready for build and debug.


Nios II C/C++ - main.cpp - Nios II IDE
File Edit Refactor Navigate Search Project Tools Run Window Help
Nios II C/C++
Nios II C/C++ Projects
altera.components
ciii_vdk_pip_demo
Binaries
Includes
Debug
cyclone3c120_config.h
i2c.h
Mixer.hpp
Scaler.hpp
Vipcore.hpp
cyclone3c120_config.c
i2c.c
main.cpp
application.stf
readme.txt
ciii_vdk_pip_demo_syslib [system]
main.cpp
/*
* main.cpp
*
* CIII VDK 1080P PiP demo software
*
* All rights reserved. Property of Bitec
* Restricted rights to use, duplicate or
* granted through contract.
*
* Copyright Bitec Ltd 2008
*
*/
#include <system.h>
#include "cyclone3c120_config.h"
#include "Mixer.hpp"
void delay(unsigned int delay)
{
for(unsigned int i=0; i < delay ; i++)
Outline
system.h
cyclone3c120_config.h
Mixer.hpp
delay
main
Make Targets
ciii_vdk_pip_demo
ciii_vdk_pip_demo_syslib
Console
Properties
C-Build [ciii_vdk_pip_demo]
Info: 9048 Bytes free for stack + heap.
Post-processing to create onchip_mem.hex
Hardware simulation is not enabled for the target SOPC Builder system. Skipping creation of hardware simulation model contents and simulation symbol files. (Note: This does not affect the instruction set simulator.)
Build completed in 10.89 seconds

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