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DSP Solutions for Industry & Research

HSMC QUAD VIDEO Mosaic Reference Design

Version 1.0

Revision history

Version	Comment
V1.0	First release

Introduction

A reference design is included with the quad video board shown in the Figure below. The design displays a mosaic of the four input channels on the DVI output port in VGA resolution (640x480). The four video input channels are first analysed and the vertical blank, pixel clock and field signal are extracted from the BT565 data stream. The YcrCb data is de-multiplexed before being transformed into a RGB565 colour space. The RGB data is then fed into the SoPC cores which transfer into the Nios II main memory. The TVP5154 scalar is programmed to reduce the input signal to QVGA size. The core DMA engine is designed to transfer the image into the correct position in memory for a mosaic effect.

A VGA core is included which transfers the image from main memory to the DVI output device. Details of this core can be found in the accompanying RTL files. The main VGA clock is derived from a PLL. The PLL also generates a 90deg phase shifted clock signal to drive the Chrontel device needed for the DDR bus operation.

A i2c core is needed to programme the video input and output devices. Details of the various internal registers can be found in the relevant device datasheets.

The jumper settings assume a composite signal is being fed into the video input channels. The input filter settings should be bypassed for composite operation. The output signal can be viewed by using either the DVI or RGB outputs. When RGB outputs are views the RGB jumpers must be set accordingly.

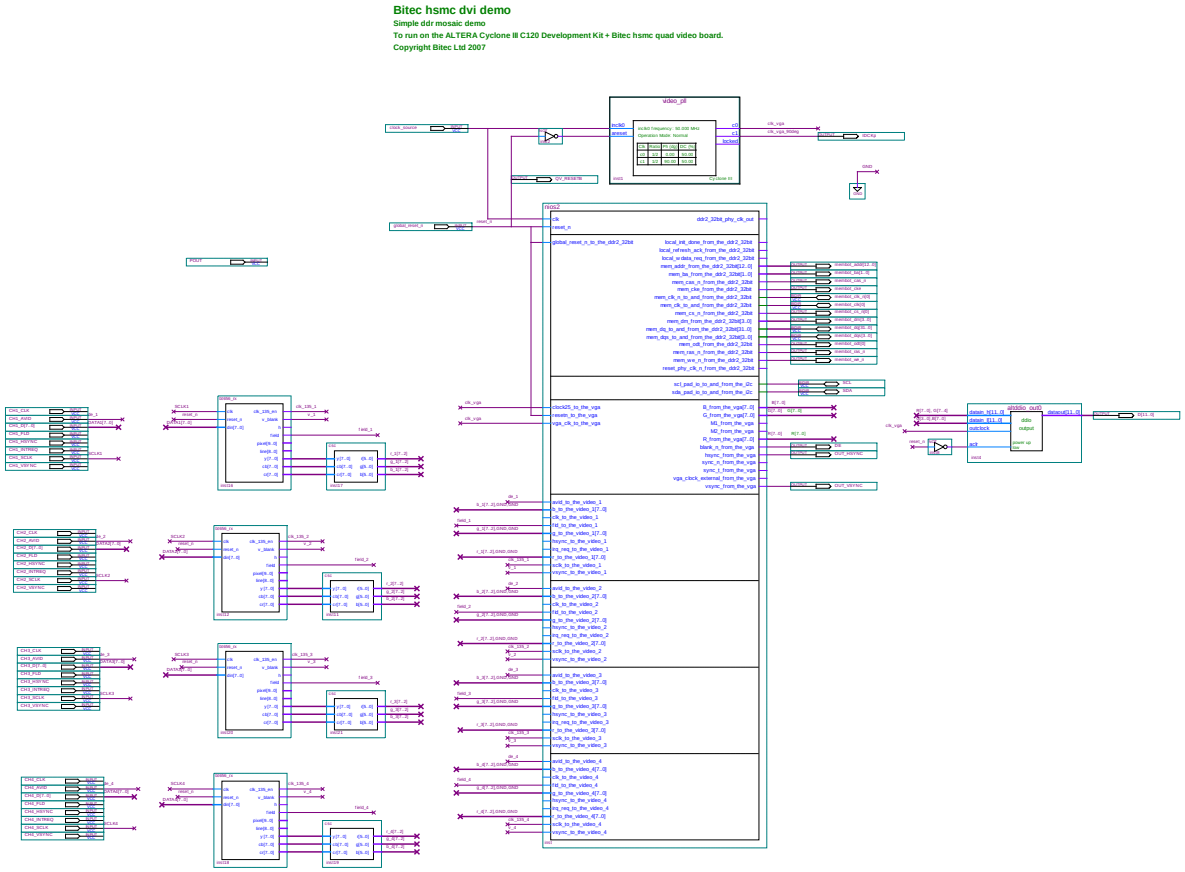


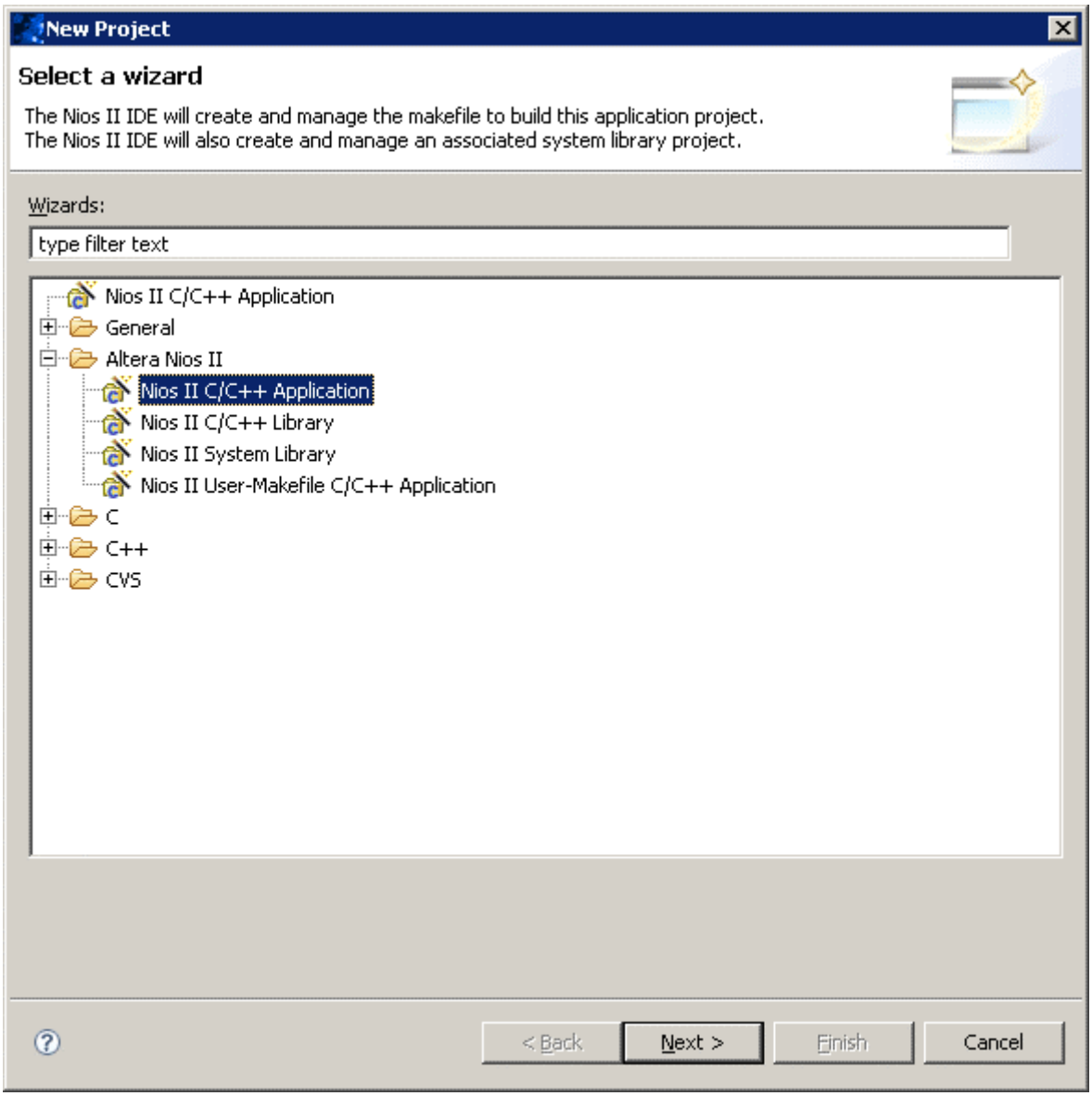
Figure 1 SoPC top level diagram.

Building the demo software

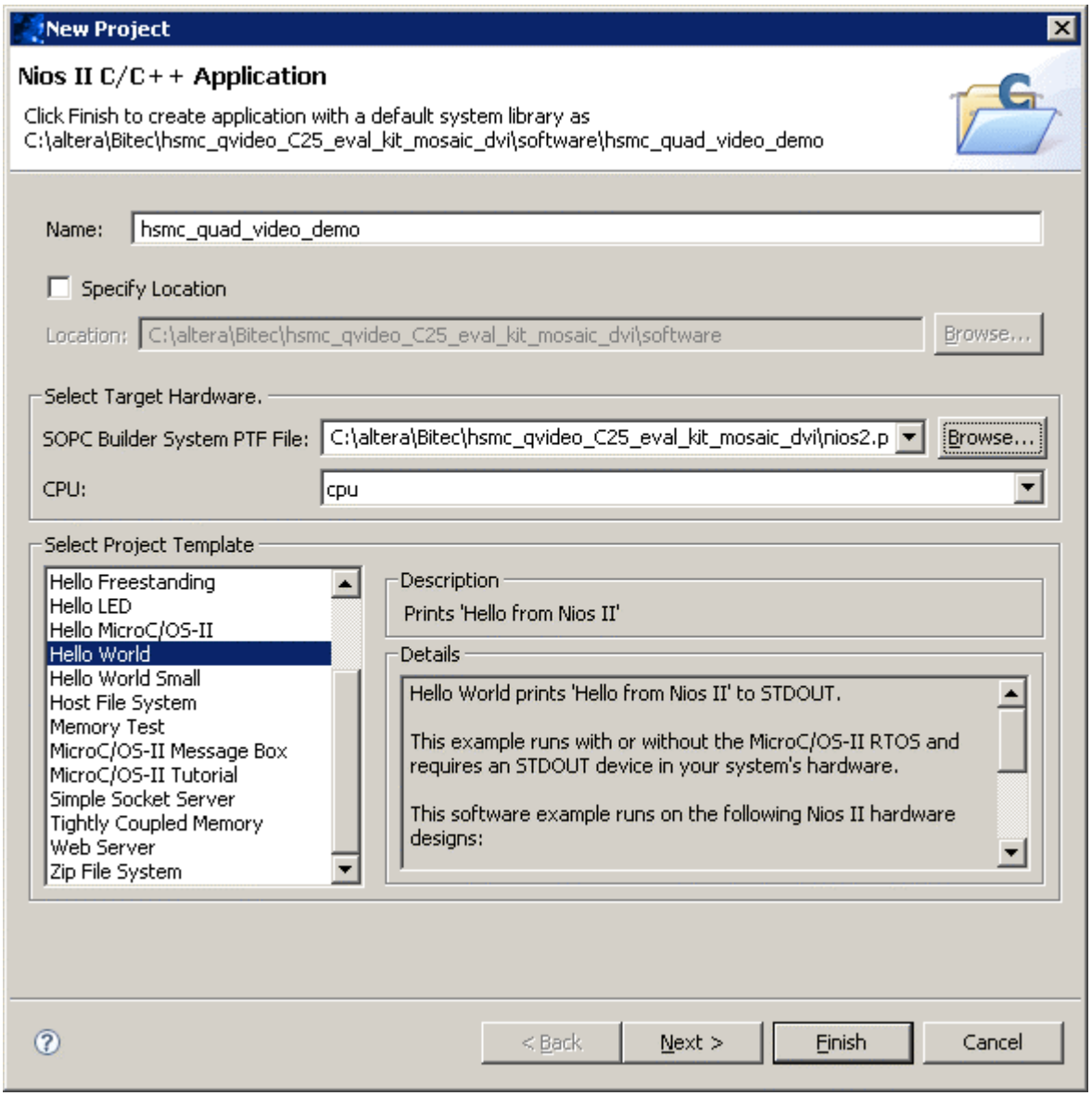
Before executing the demo software it is first necessary to create a Nios II project and include the supplied source files.

Open the Nios II IDE and “Switch Workspace” to the “Software” directory.

Create a new “Nios II C/C++ Application” from the File->New menu.



Change the project name to hsmc_quad_video_demo and choose the SOPC Builder System PTF to select the Quad Video demo Nios II processor description file.



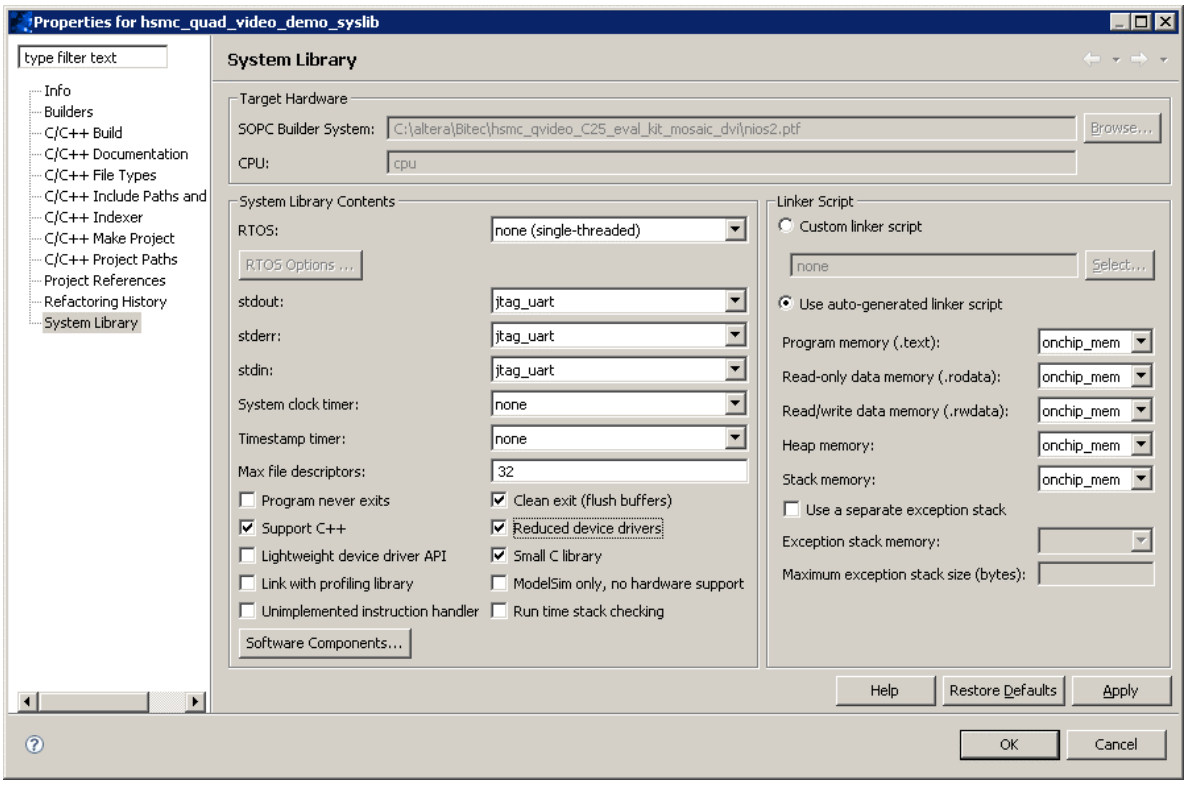
Click “Next” and then “Finish”. Two directories will be created below the Software directory.

Copy the supplied source files into the newly created “hsmc_quad_video_demo” directory.

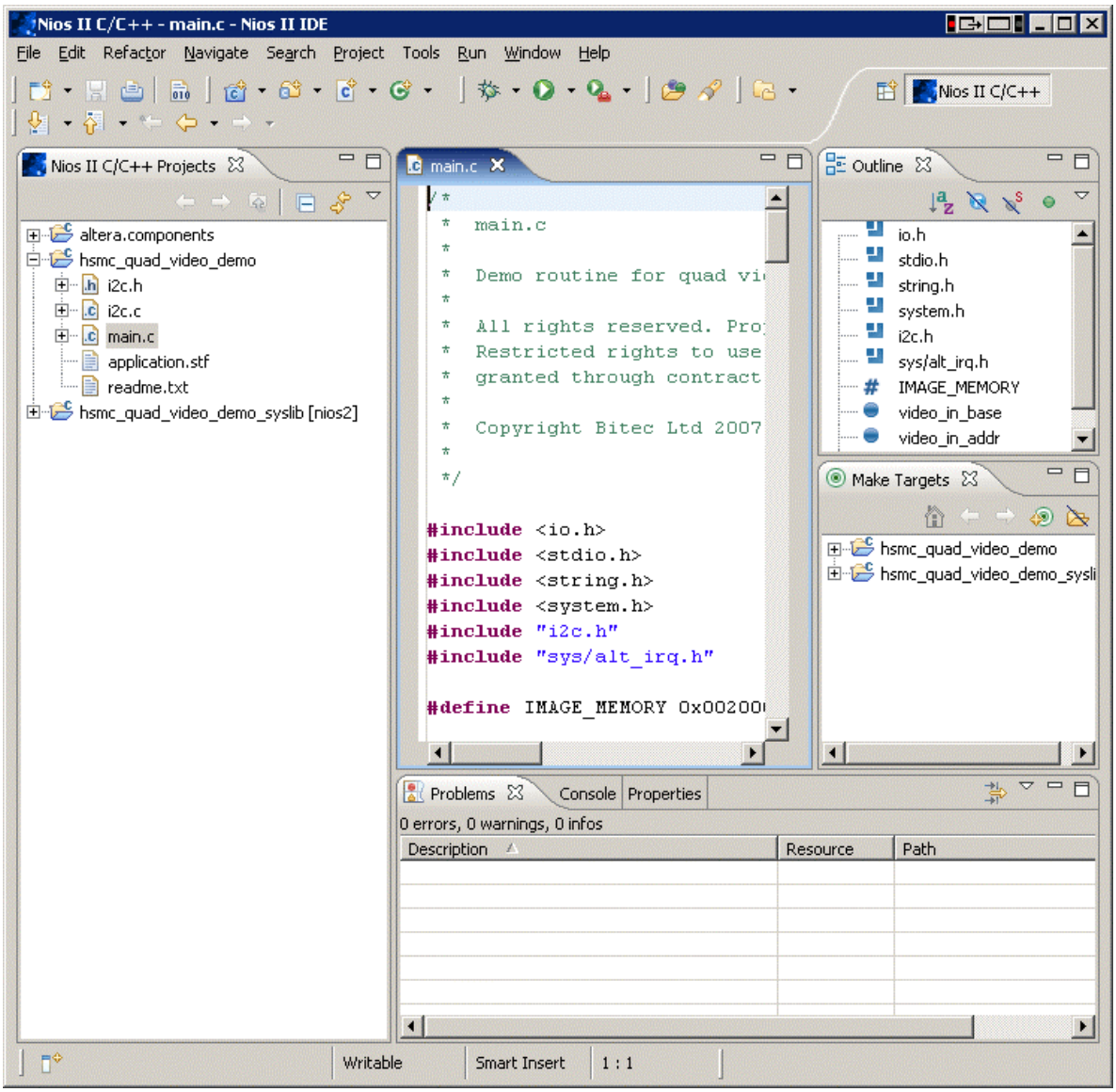
Highlight the hsmc_quad_video_demo directory in “Project Browser” pane “Refresh” using F5 or File->Refresh.

Select the auto generated hello_world.c and delete.

Before building, set the memory options to “onchip_mem” in the system library properties. Also select the “Reduced Drivers” and “Small C Library” options.



The project is now ready for build and debug.


Nios II C/C++ - main.c - Nios II IDE
File Edit Refactor Navigate Search Project Tools Run Window Help
Nios II C/C++
Nios II C/C++ Projects
altera.components
hsmc_quad_video_demo
i2c.h
i2c.c
main.c
application.stf
readme.txt
hsmc_quad_video_demo_syslib [nios2]
main.c
/*
* main.c
*
* Demo routine for quad vi
*
* All rights reserved. Pro
* Restricted rights to use
* granted through contract
*
* Copyright Bitec Ltd 2007
*
*/
#include <io.h>
#include <stdio.h>
#include <string.h>
#include <system.h>
#include "i2c.h"
#include "sys/alt_irq.h"
#define IMAGE_MEMORY 0x00200
Outline
io.h
stdio.h
string.h
system.h
i2c.h
sys/alt_irq.h
IMAGE_MEMORY
video_in_base
video_in_addr
Make Targets
hsmc_quad_video_demo
hsmc_quad_video_demo_sysli
Problems
Console
Properties
0 errors, 0 warnings, 0 infos
Description
Resource
Path
Writable
Smart Insert
1 : 1

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