

*HSMC DVI 1080P Colour-Space  
Conversion Reference Design*

Version 0.1



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## Revision history

Version	Comment
V0.1	Beta release

## Introduction

Colour space conversion is the translation of the representation of a colour from one basis to another. This typically occurs in the context of converting an image that is represented in one colour space to another colour space, the goal being to make the translated image look as similar as possible to the original.

The Colour-Space conversion reference design extends the SDRAM Loop-through demo by adding a standard RGB-YCrCb colour space conversion. Such an operation is typical for HD 1080P systems that convert from computer RGB to HDMI graphics based systems.

A schematic of the demo is shown below in Figure 1. The CSC block accepts the output video stream and performs a RGB to Y Cr Cb colour conversion. The new video stream is then sent to the DVI port for connection to a monitor or TV via a DVI-to-HDMI converter cable.

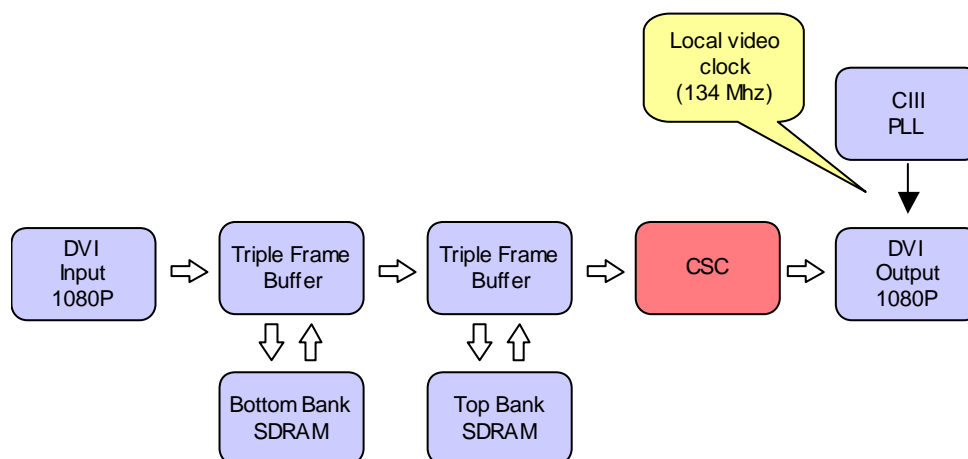


Figure 1

The SoPC builder is shown below. The two DDR2 memory banks run at 166Mhz and the local SoPC system clock is set to the bottom bank sys clock to avoid the need for two clock crossing bridges.

Details of the individual components can be found in the Altera VIP documentation.

The Colour-Space converter is highlighted with its corresponding connections to the Avalon fabric. The CSC block is clocked at the same rate as the video pipeline.

Name	Source	MHz
clk	External	125.0
ddr2_32bit_bot_sysclk	ddr2_32bit_bot.sysclk	166.0
ddr2_32bit_bot_auxfull	ddr2_32bit_bot.auxfull	166.0
ddr2_32bit_bot_auxhalf	ddr2_32bit_bot.auxhalf	83.0

Use	Connections	Module Name	Description	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>		vga_in_inst	Clocked Video Input	ddr2_32bit_bot_sysclk			
<input checked="" type="checkbox"/>		my_alt_vip_vfb_bot	Frame Buffer	ddr2_32bit_bot_sysclk			
<input checked="" type="checkbox"/>		ddr2_32bit_bot	DDR2 SDRAM High Performance Contr...	clk	0x00000000	0x07ffffff	
<input checked="" type="checkbox"/>		my_alt_vip_vfb_top	Frame Buffer	ddr2_32bit_bot_sysclk			
<input checked="" type="checkbox"/>		clock_crossing_brid...	Avalon-MM Clock Crossing Bridge	ddr2_32bit_bot_sysclk	0x00000000	0x07ffffff	
<input checked="" type="checkbox"/>		ddr2_32bit_top	DDR2 SDRAM High Performance Contr...	clk	0x00000000	0x07ffffff	
<input checked="" type="checkbox"/>		my_alt_vip_csc	CSC	ddr2_32bit_bot_sysclk			
<input checked="" type="checkbox"/>		vga_out_inst	Clocked Video Output	ddr2_32bit_bot_sysclk			

Figure 2

## Installation

To run the design it is first necessary to obtain the source files and restore the Quartus Archive (QAR) file into a chosen directory.

A 1080P video source and capable display is required to run the demonstration. For correct operation it is necessary to configure the video test signal to have positive polarity on both the vertical and horizontal sync signals.

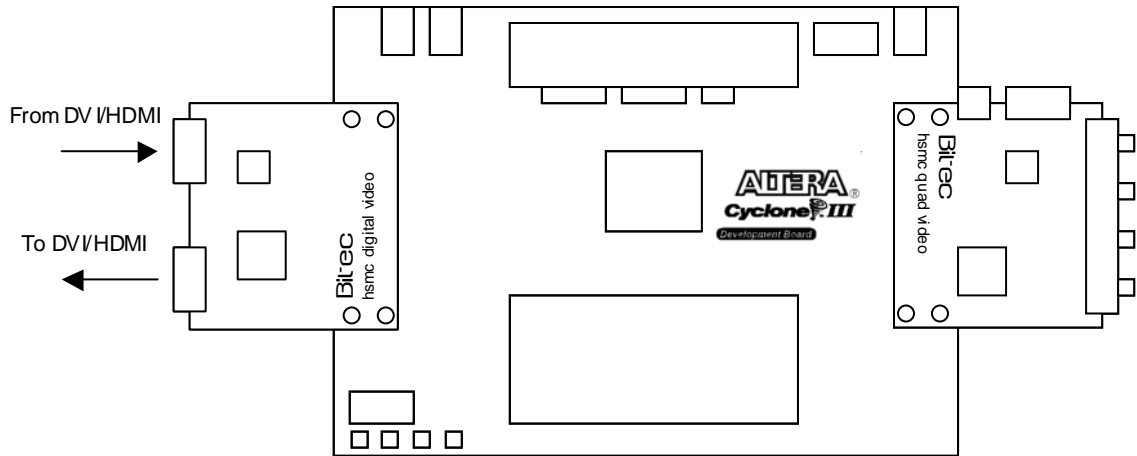


Figure 3

Once the hardware and software are ready, the sof file must be downloaded into the target Dev Kit board.

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