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DSP Solutions for Industry & Research

CIII VDK Optrex LCD Reference Design

Version 0.1

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Revision history

Version	Comment
V0.1	Beta release

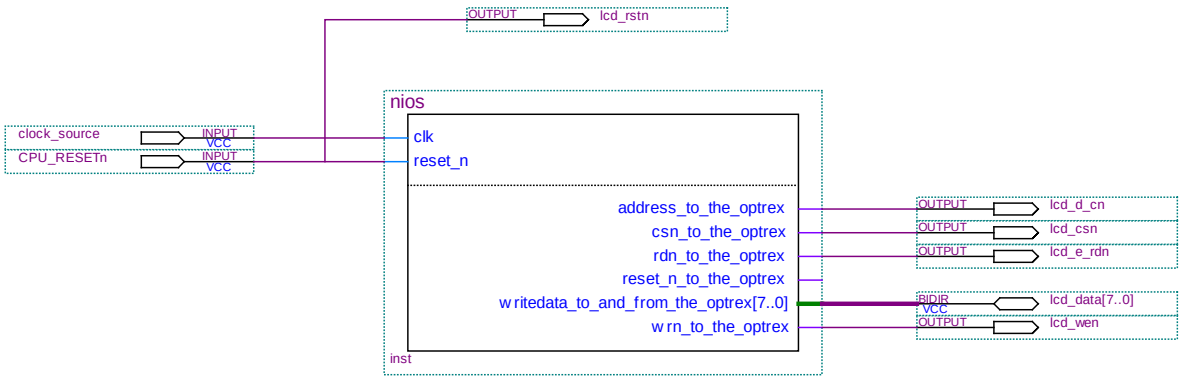
Introduction

The Monochrome Optrex LCD screen on the CIII Dev Kit allows developers to include low resolution user feedback in their designs. This demo displays a checker-board on the display.

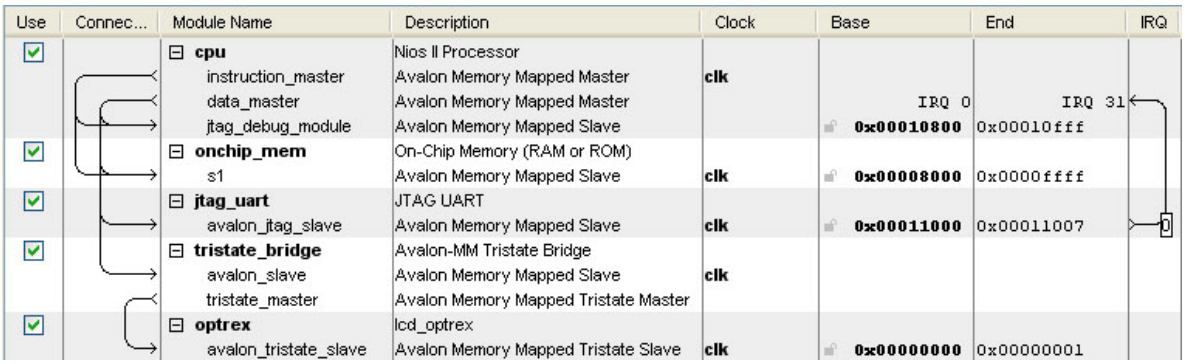
Two documents are included in the design that describe in details the hardware and software aspects of the Optrex device. This reference design is based on the information in these documents. The reader is referred to these documents for information on programming the Optrex device.

In this design, a Nios II processor drives the Optrex device. The Nios II must write all information displayed on the LCD screen. Details of register access and programming techniques can be found in the accompanying Optrex data.

The top-level diagram is shown below. The design uses a simple Nios II processor to drive the Optrex display via a Avalon slave device inside SoPC.

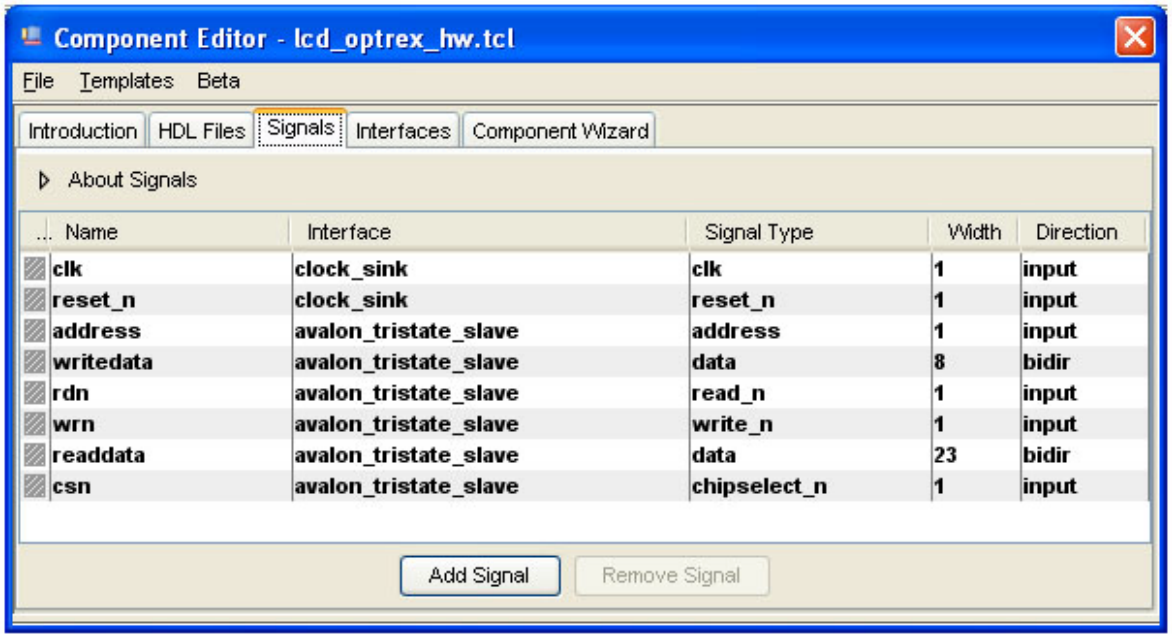


The internal SoPC component structure is shown below. A tri-state bridge is necessary to drive the bi-directional Optrex data signals.



Use	Connec...	Module Name	Description	Clock	Base	End	IRQ
☑		**cpu**	Nios II Processor				
		instruction_master	Avalon Memory Mapped Master	**clk**			
		data_master	Avalon Memory Mapped Master			IRQ 0	IRQ 31
		jtag_debug_module	Avalon Memory Mapped Slave		**0x00010800**	0x00010fff	
☑		**onchip_mem**	On-Chip Memory (RAM or ROM)				
		s1	Avalon Memory Mapped Slave	**clk**	**0x00008000**	0x0000ffff	
☑		**jtag_uart**	JTAG UART				
		avalon_jtag_slave	Avalon Memory Mapped Slave	**clk**	**0x00011000**	0x00011007	0
☑		**tristate_bridge**	Avalon-MM Tristate Bridge				
		avalon_slave	Avalon Memory Mapped Slave	**clk**			
		tristate_master	Avalon Memory Mapped Tristate Master				
☑		**optrex**	lcd_optrex				
		avalon_tristate_slave	Avalon Memory Mapped Tristate Slave	**clk**	**0x00000000**	0x00000001	

The Optrex component is a simple Avalon Slave device with no RTL code. The Avalon signals are automatically exported and should be connected to the hardware pins as shown in the top-level diagram.

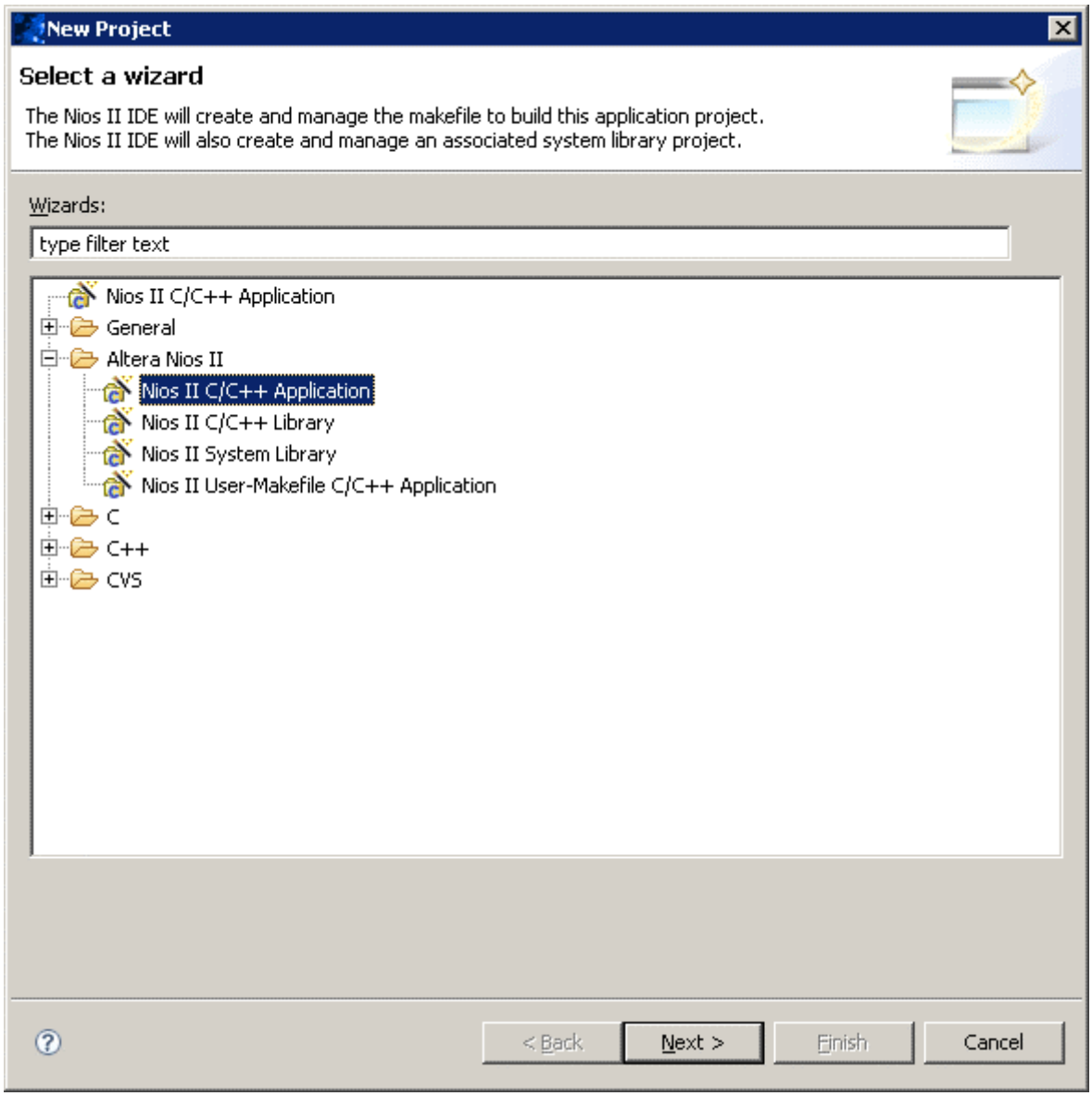


Re-building the software

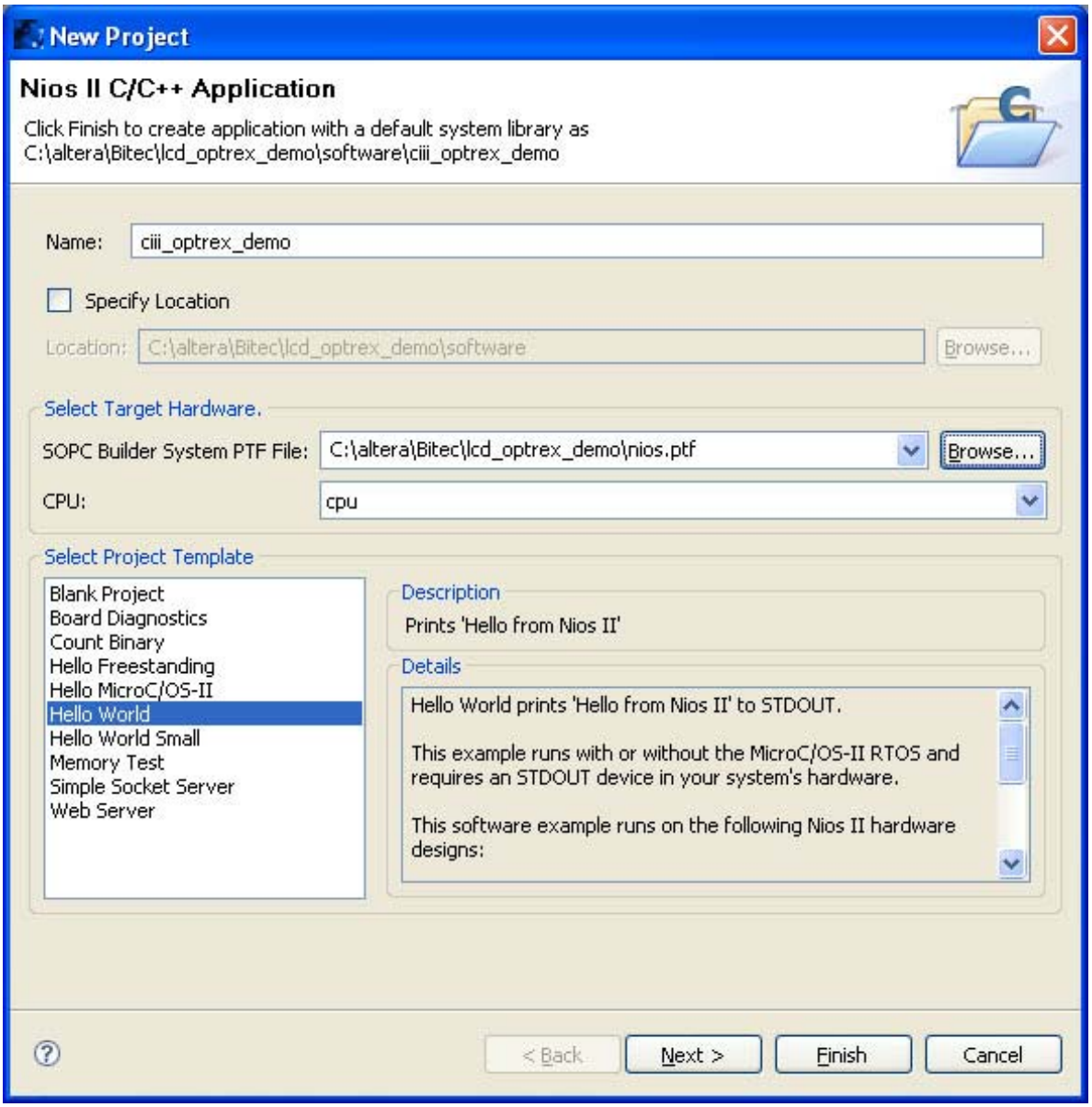
Before executing the demo software it is first necessary to create a Nios II project and include the supplied source files.

Open the Nios II IDE and “Switch Workspace” to the “Software” directory.

Create a new “Nios II C/C++ Application” from the File->New menu.



Change the project name to ciii_optrex_demo and choose the SOPC Builder System PTF to select the niosii.ptf demo Nios II processor description file.



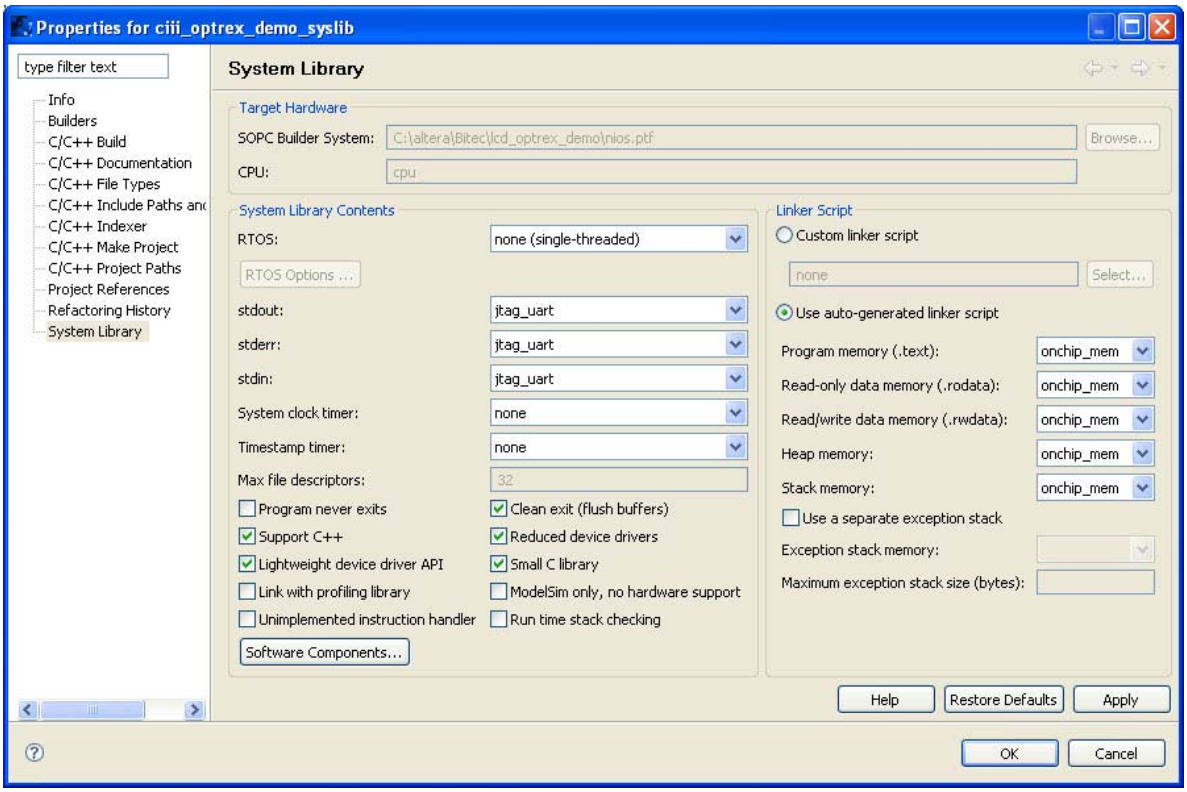
Click “Next” and then “Finish”. Two directories will be created below the Software directory.

Copy the supplied source files into the newly created “ciii_optrex_demo” directory.

Highlight the ciii_optrex_demo directory in “Project Browser” pane “Refresh” using F5 or File->Refresh.

Select the auto generated hello_world.c and delete.

Before building, set the memory options to “onchip_mem” in the system library properties. Also select the “Reduced Drivers” and “Small C Library” options.



The demo design can now be debugged in hardware.

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