Bitec

DSP Solutions For Industry & Research

Product Brief : DisplayPort 1.4 IP Core

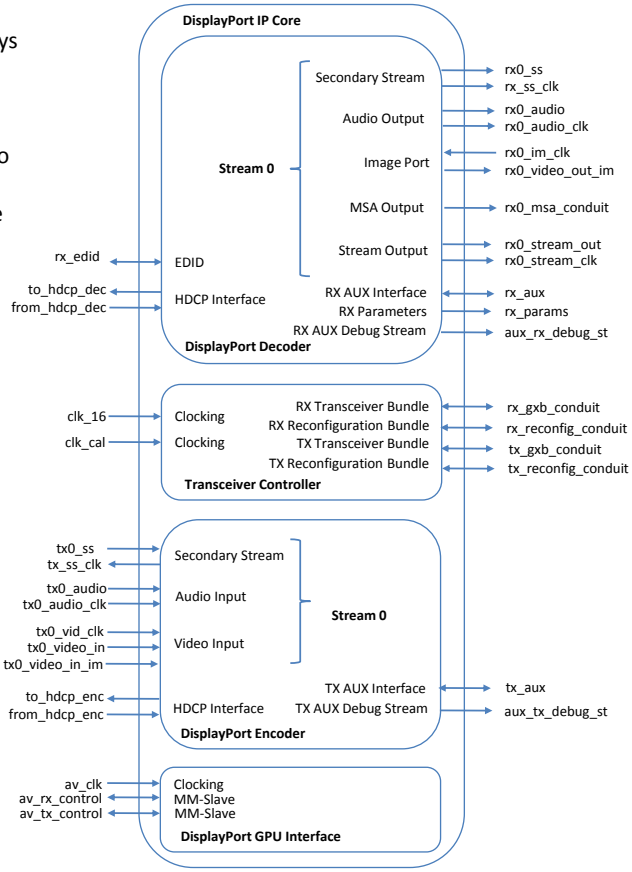
DisplayPort heralds a new alternative in video connectivity. Designed to enable low cost direct drive monitors and backed by industry leaders (Intel, DELL, Apple etc) DisplayPort is not hindered by license and royalty fees.

The Bitec DisplayPort IP core for FPGA and ASIC devices offers a cost-efficient industry leading solution to rapidly develop and deliver displays offering a superior viewing experience within ever-shrinking product lifecycles.

The Bitec DP IP core accepts 1,2 or 4 lanes at rates between 1.62GB/s to 8.1GB/s link rate. In accordance with the DP specification 1.4, the core will adapt and train to the transmitting source capability via a firmware driven policy maker API.

The source and sink cores accept v/h/d-sync and parallel RGB data. Audio data and raw Auxiliary data ports to the cores provide flexible side-band messaging.

Bitec also offer a tailoring service for bespoke designs. For more information contact Bitec.



Features

- **Feature rich parametrization for optimal designs**
- **Efficient clock resource usage**
- **Support for 1,2 & 4-lane**
- **Support DisplayPort 1.4**
- **Support 1.62 to 8.1Gbps link rate (includes eDP rates)**
- **Dual/quad symbol modes**
- **Versatile PMA/PHY interface**
- **Single/dual/quad pixel modes**
- **6,8,10,12 & 16 bit color support**
- **Multi bus support register control interface**
- **Supports RGB, YCbCr Colorimetric Formats (444,422,420)**
- **Support RAW and Y-only color formats**
- **Autonomous AUX channel or GPU driven**
- **AUX debug channel**
- **Optional HDCP 2.2/1.3 Support**
- **8-Channel Audio**
- **Adaptive-Sync support**
- **Forward Error Correction**
- **eDP Features supported**
- **Optional DSC support**
- **Optional Pixel Clock Recovery implementation**
- **Full, portable API in C-language for policy layer**

Contact info@bitec-dsp.com for more information

Supported Technology

- MicroSemi PolarFIRE FPGA
- Lattice ECP5 FPGAs
- Altera GXB FPGAs
- ASIC

Deliverables

- Encrypted or source code DP 1.4 IP
- Binary or source code API libraries
- Documentation
- FPGA Example designs

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